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PRESS RELEASE

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FOR IMMEDIATE RELEASE

### **Zocalo Tech, Inc. Introduces First EDA Tool Dedicated to Assertion Library Productivity**

Austin, TX, February 16, 2009 -- Zocalo Tech, Inc., an Austin, Texas startup, is introducing Zazz at DVCon 2009. Zazz is a productivity tool for use with assertion libraries. The initial release supports Accellera's Open Verification Library (OVL) and Cadence's Incisive<sup>®</sup> Assertion Library (IAL).

Dave Stevens, Vice President of Operations explains, "For designers the availability of assertion libraries has special importance since they address most designer assertion checker needs. Assertion checkers added by the designer during the design cycle can have significant impact on detecting problems early in the functional verification process. The designer knows the intent of the design, formal verification is enabled and communication is increased between designers and verification engineers. The availability of assertion libraries represents an advancement in assertion-use productivity. Zazz makes using assertion libraries quick and easy by automating the tedious error-prone tasks via an easy to use intuitive GUI."

"The value of enabling designers to add and manage assertions easily is clear," said Michal Siwinski, Group Director of Enterprise Verification at Cadence<sup>®</sup> Design Systems, Inc. "Zazz provides the designer community significant productivity gains and ease of use over manual instantiation of assertion checkers, leveraging the Incisive<sup>®</sup> Assertion Library in their flow. We are pleased that Zocalo is helping more designers to add assertions and reap the benefits of assertion-based verification."

Zazz is a SystemVerilog based tool supporting any mix of Verilog 1995, Verilog 2001 and SystemVerilog files. The basic process is described as follows:

- The design is read in and automatically parsed for display.
- The user graphically selects the assertion of choice and attaches it to the appropriate design element in the design hierarchy view.
- Parameters with predefined valid values are entered from an enumerated drop down menu or custom defined without regard to sequence or format.
- Port expressions may be created quickly by selecting from a filtered list of signals available in the attachment scope of the design.
- All parameter and port expressions are dynamically parsed and elaborated to ensure their validity.
- The checker and associated parameter values and port connections are then automatically documented via Zazz's auto-documentation capability.

Zazz operates in two modes. Single File mode is optimized for adding assertions checkers while the designer is defining the RTL code and thinking about the requirements and constraints as the design progresses. No project setup is required providing the ability get in and out of Zazz from their editor with a single command. Project Mode extends the ability for binding checkers to multiple design elements and provides the structure to format all of the assertion documentation in a single customizable file for inclusion in the verification plan.

The project may chose to utilize designer provided assertions in the single file mode as the design progresses and add additional assertions as major design elements (functional blocks subsystems or the entire FPGA, ASIC or SoC) are complete or choose to add all assertions when the major design elements are complete.

#### **Availability and Pricing**

Zazz will be available beginning Q2 2009 on Red Hat and Suse Linux. At that time a product demonstration and free 30-day trial will be available at [www.zocalo-tech.com](http://www.zocalo-tech.com). List price is \$4950 for a 1-year subscription supporting OVL. Introductory pricing through Q3 2009 is \$2,950. Addition of the IAL support option is \$500.

#### **About Zocalo Tech, Inc.**

Zocalo Tech, Inc. is a privately funded provider of EDA solutions focused on increased productivity for engineers adopting and utilizing Assertion Based Design and Assertion Based Verification.

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